

ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE
REPLACEMENT DRAWING

Inventor: Yoshiyuki Yanagisawa et al.
Serial No. 09/876,290
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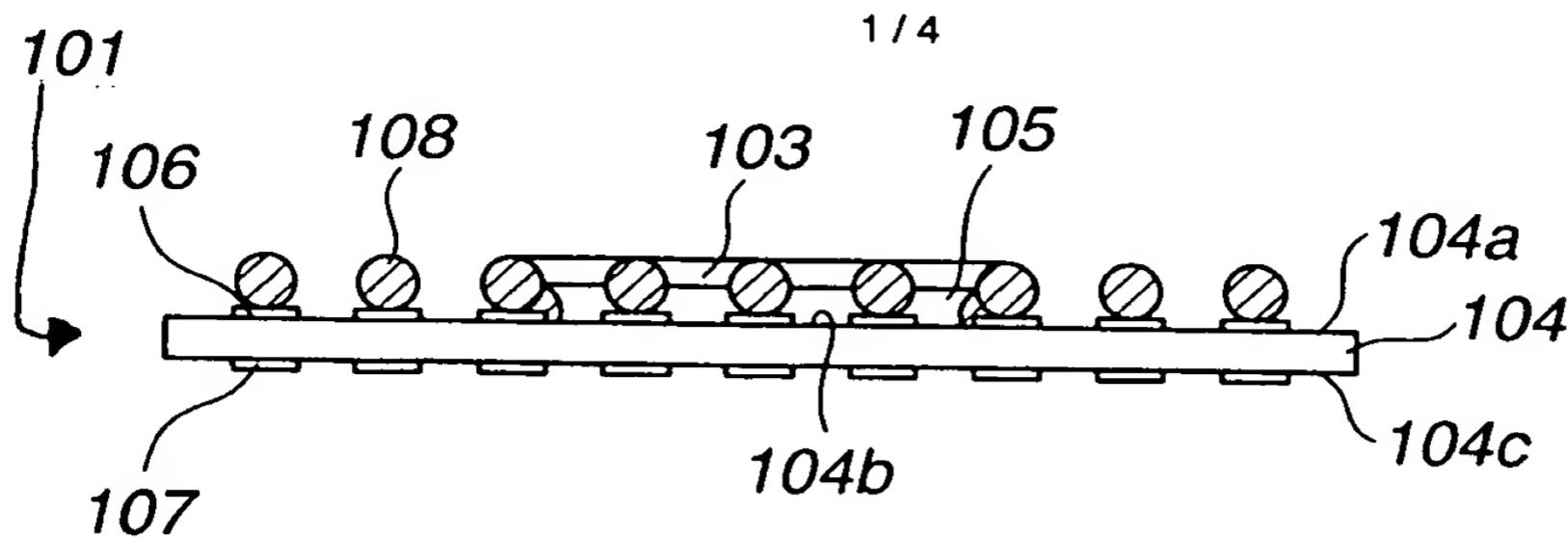


FIG. 1(a)

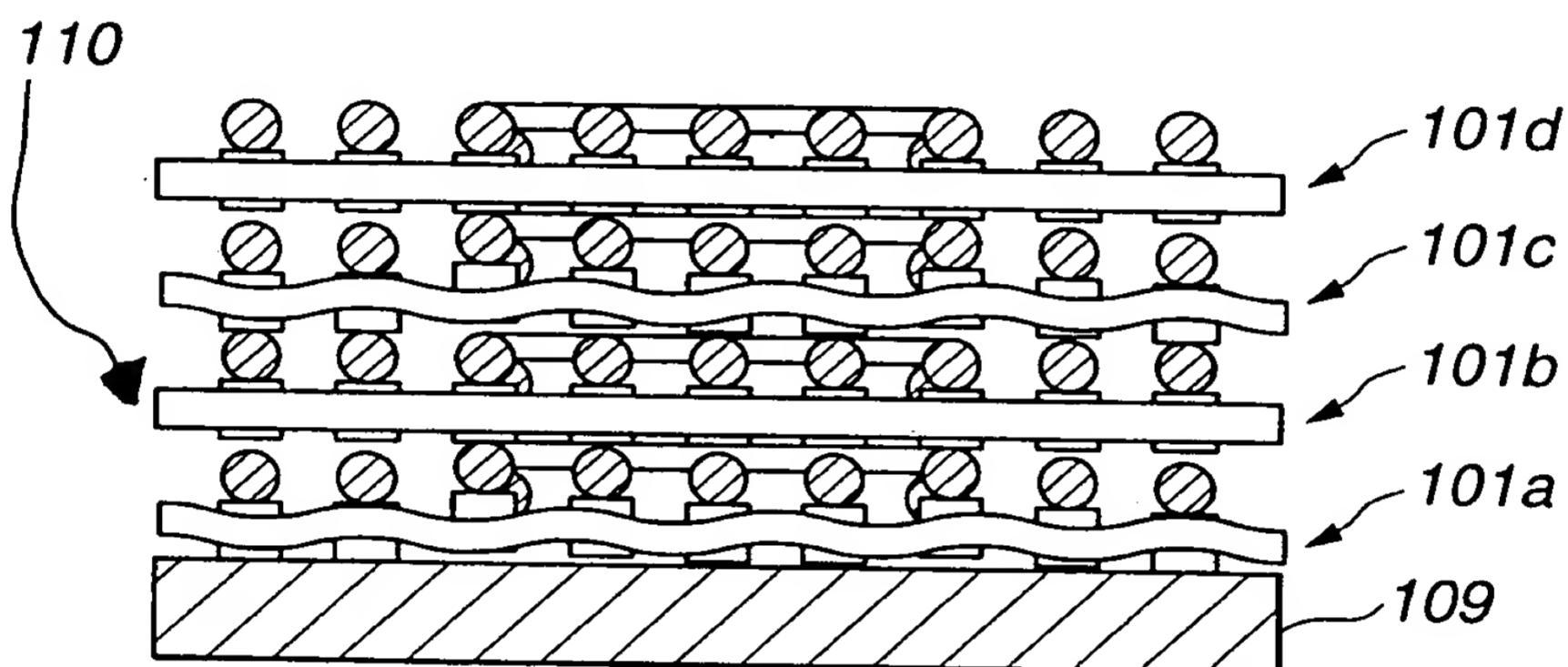


FIG. 1(b)

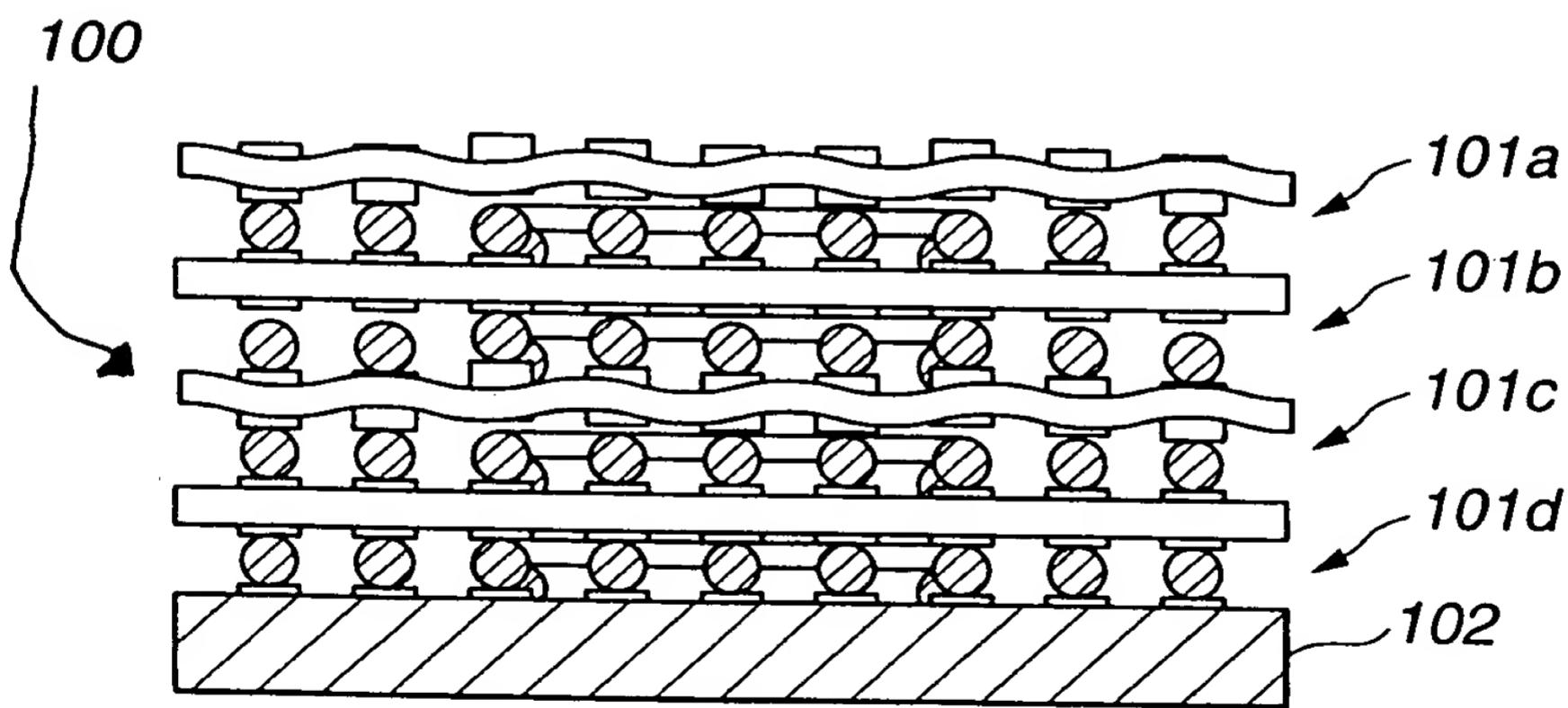


FIG. 1(c)

**ASSEMBLY JIG A
REPLACEMENT DRAWINGS**

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FIG.2(a)

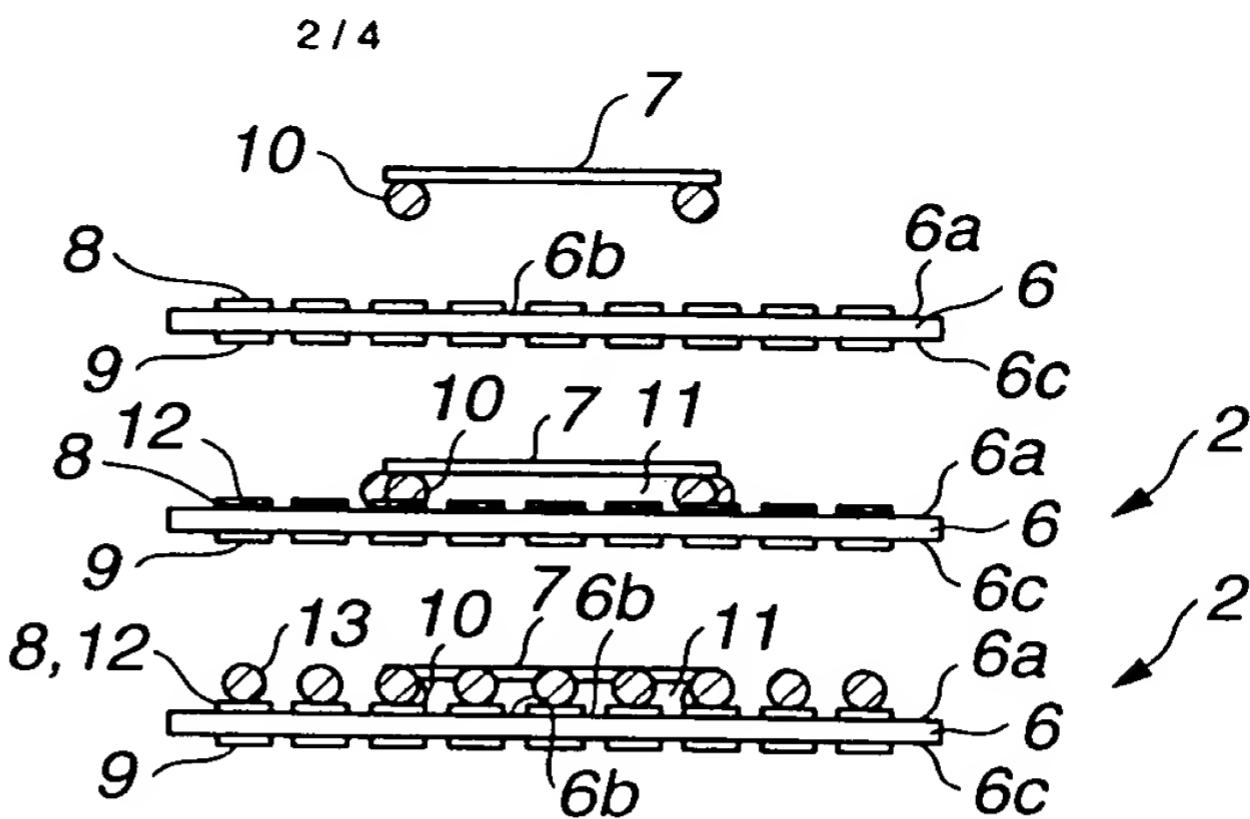


FIG.2(b)

FIG.2(c)

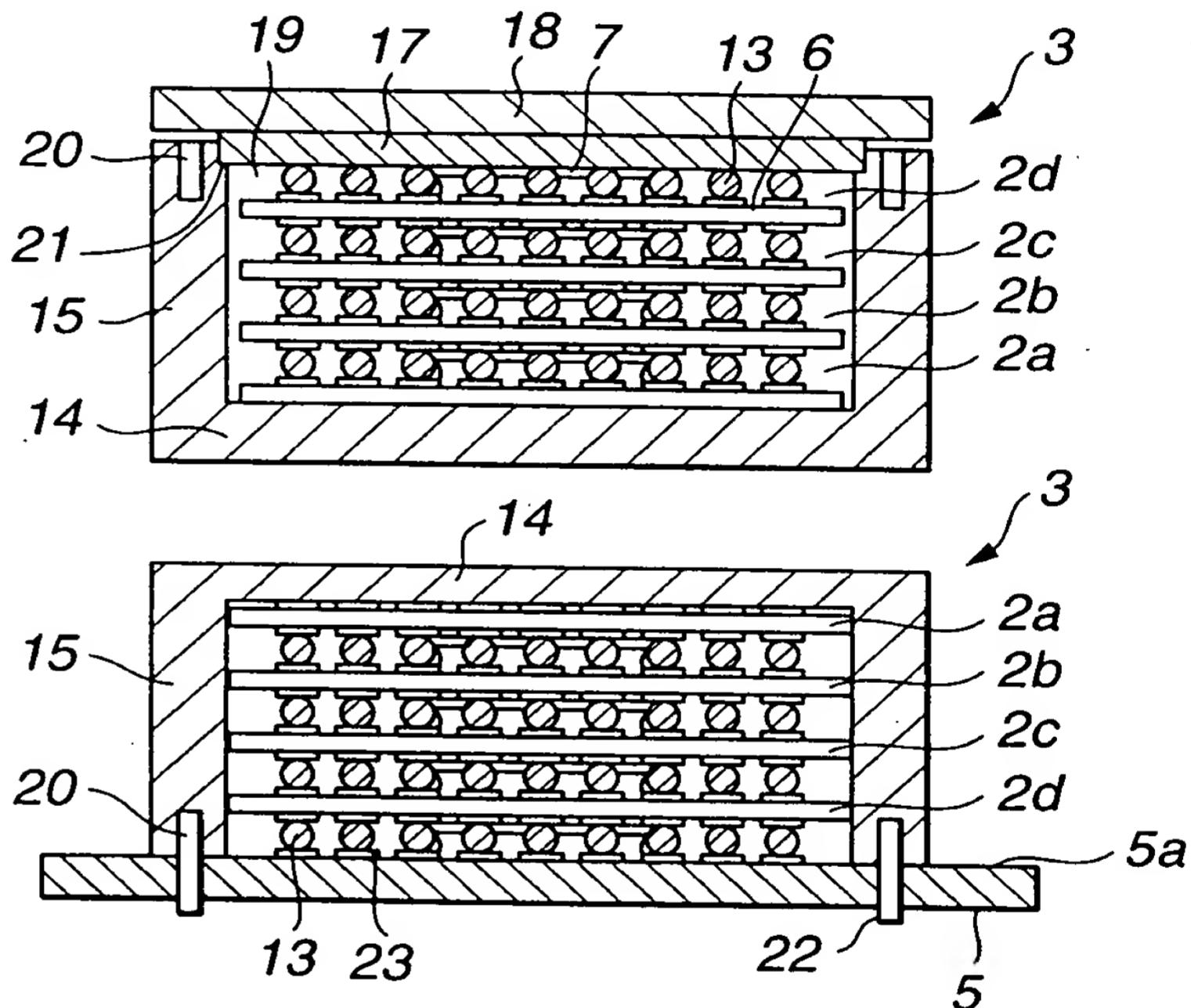
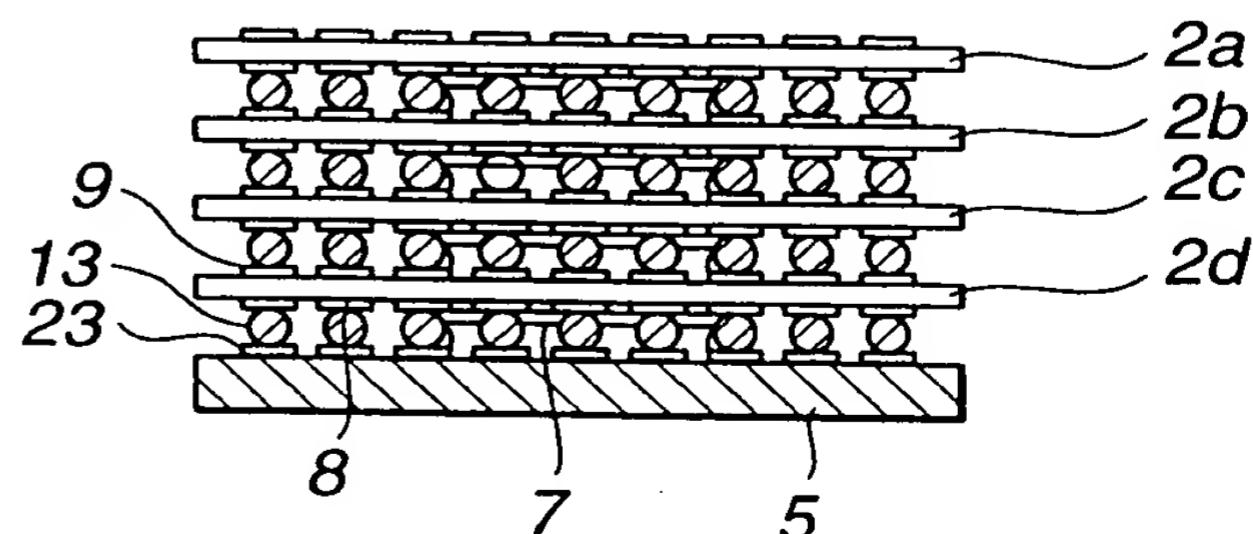


FIG.2(e)



**ASSEMBLY JIG
REPLACEMENT DRAWINGS**

STRUCTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE

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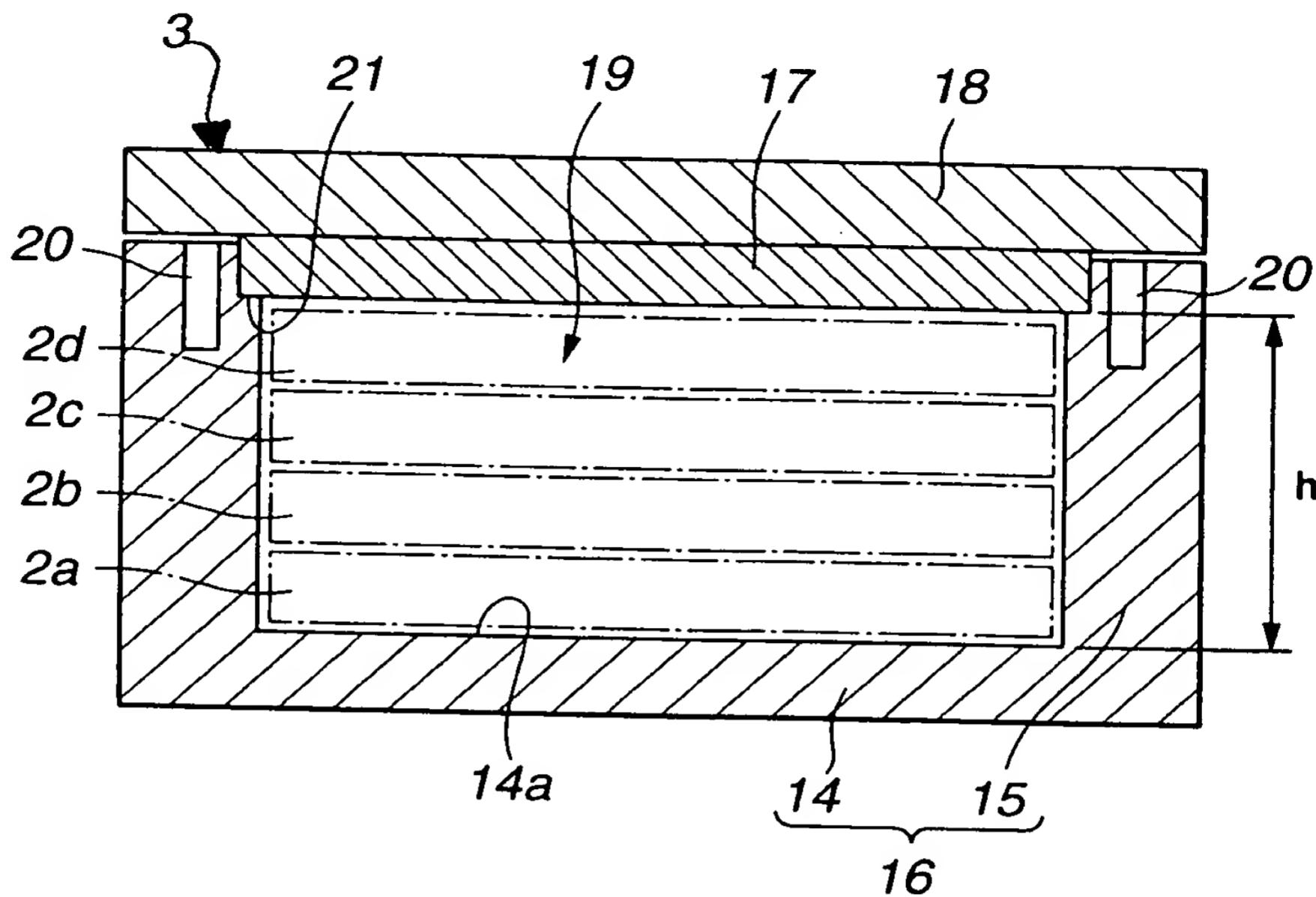


FIG.3

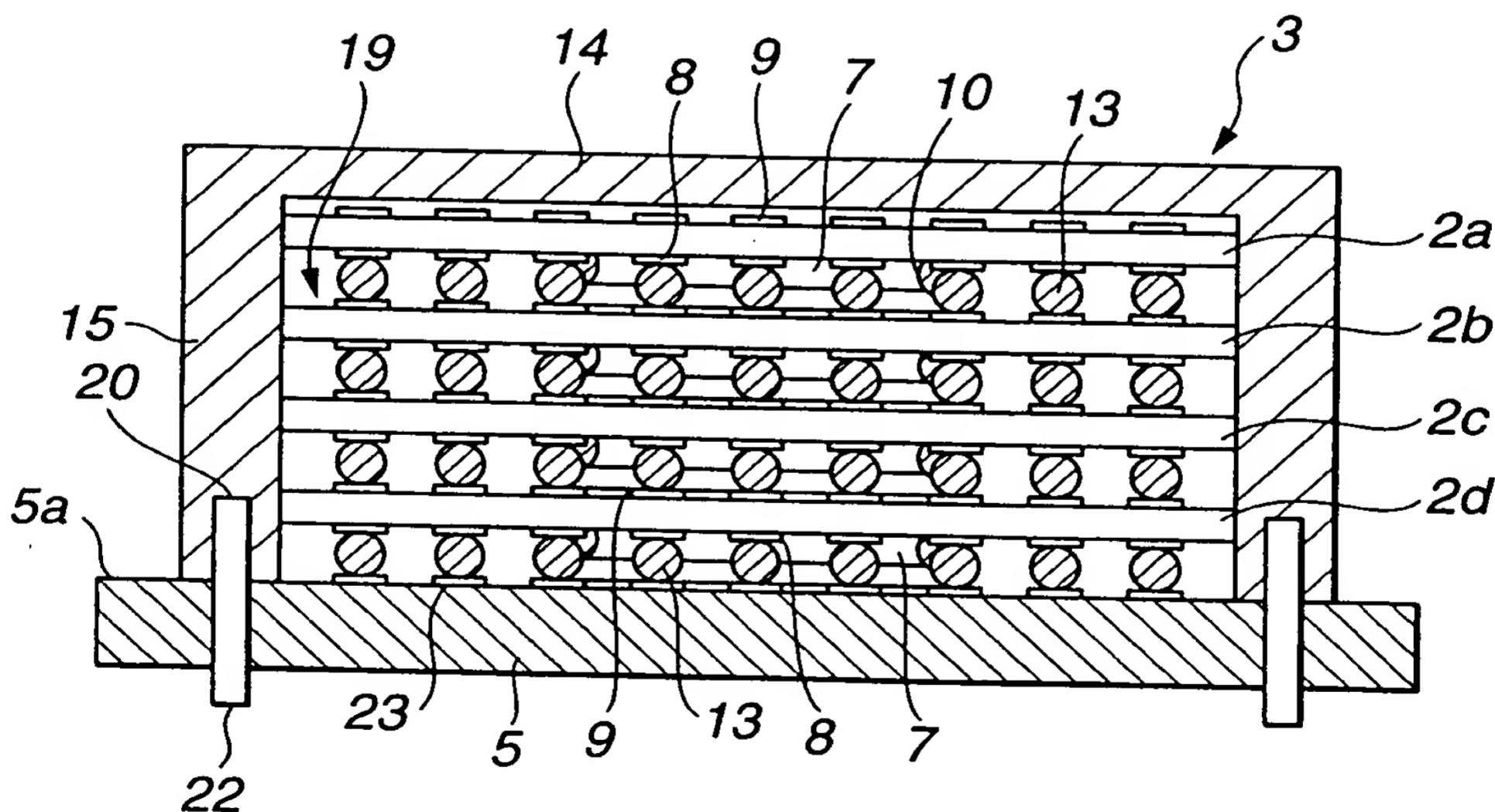


FIG.4

ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE
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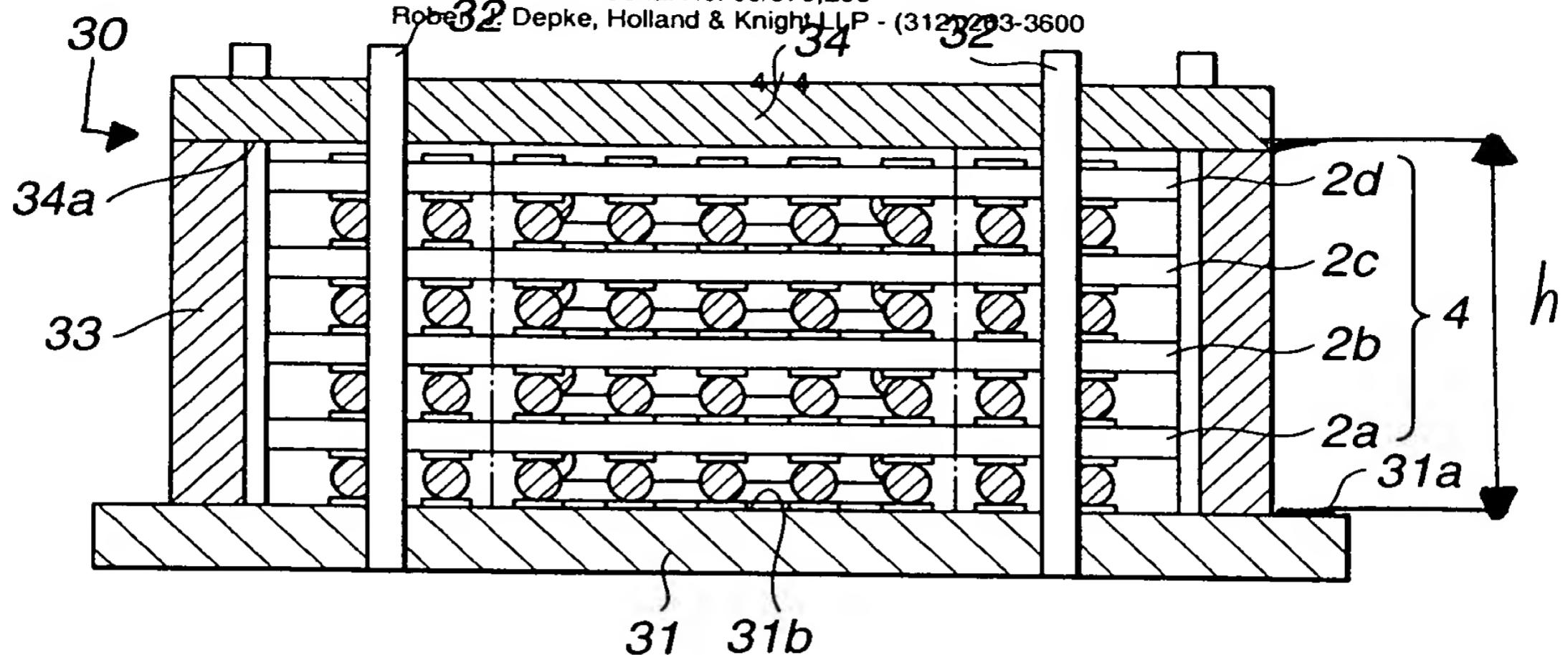


FIG.5(a)

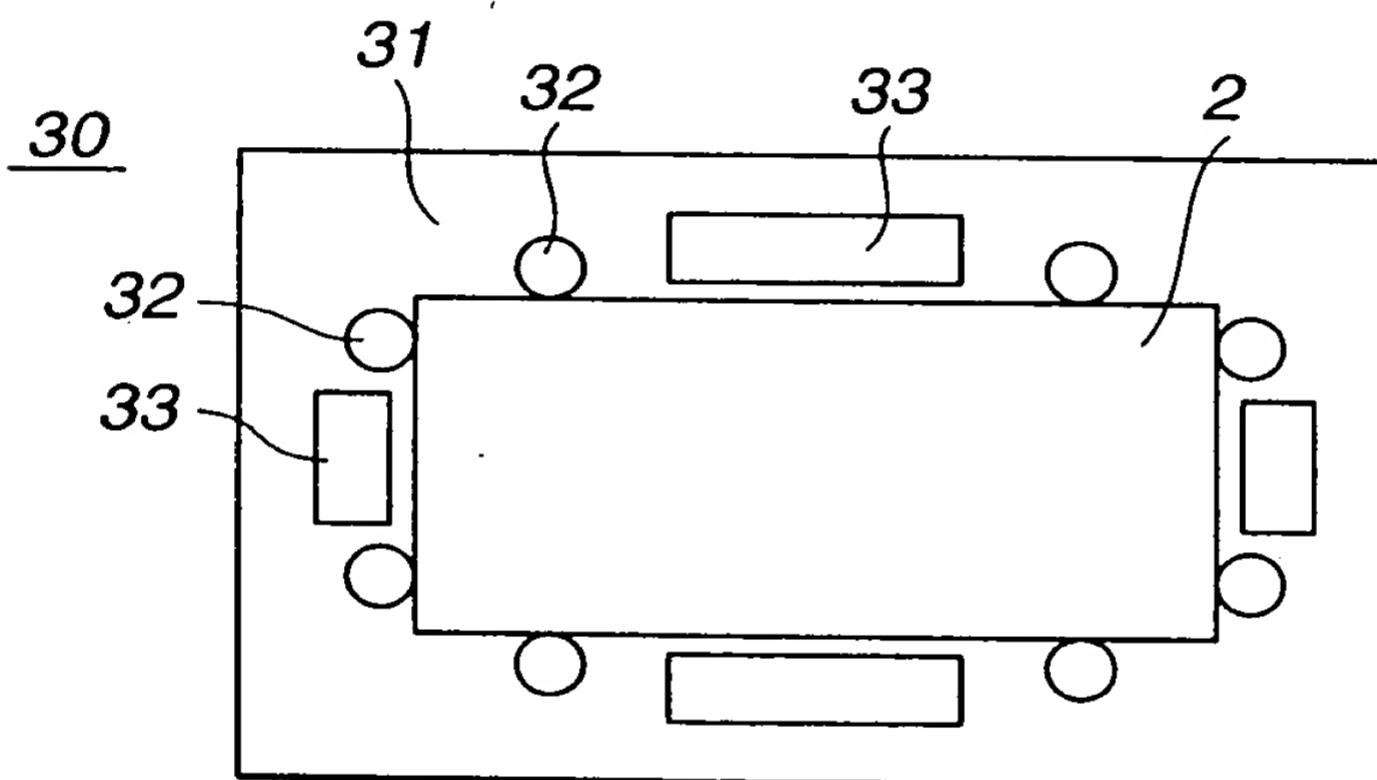


FIG.5(b)

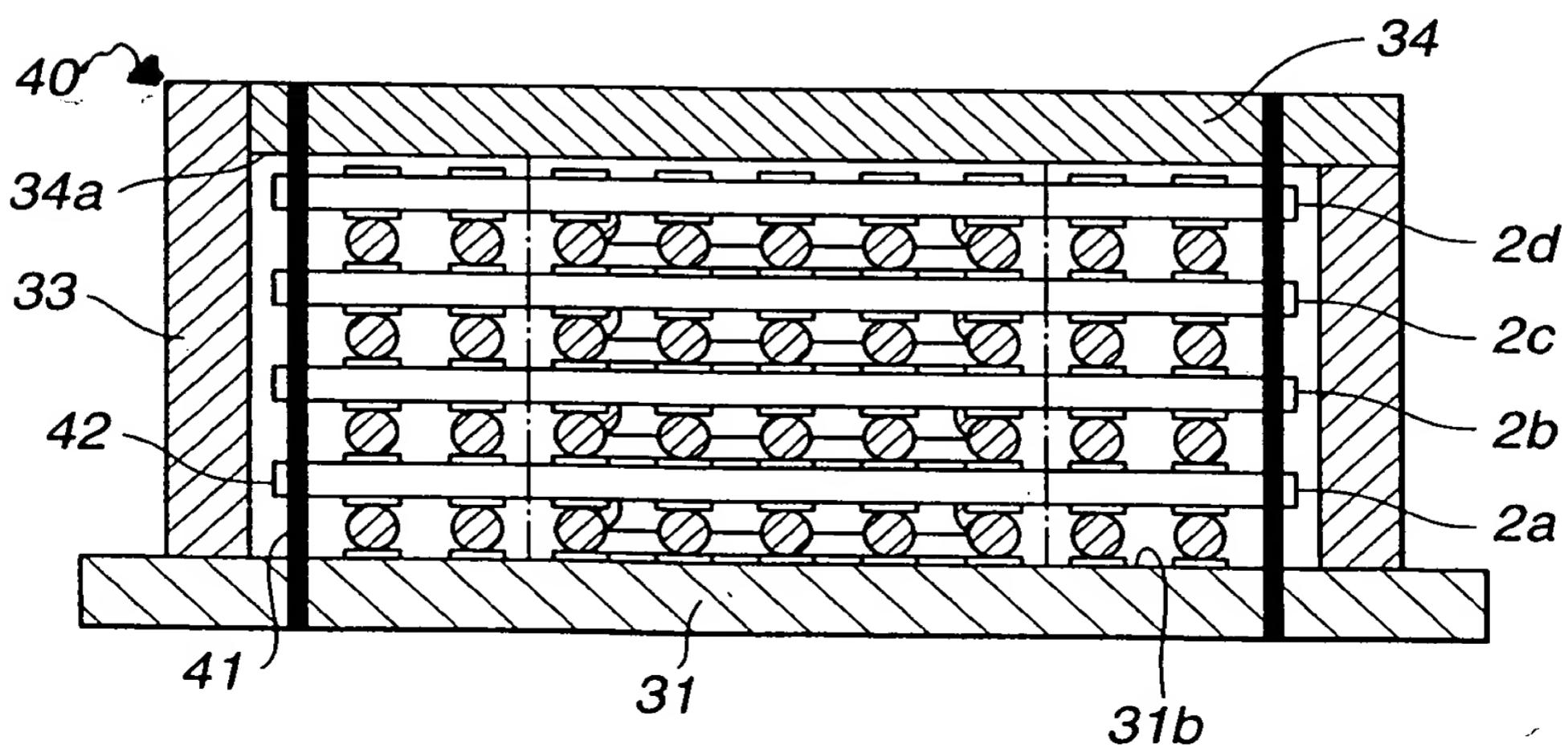


FIG.6